TR-82-008

INTEGRATED COMPUTER ARCHITECTURE FOR PATTERN ANALYSIS AND IMAGE DATABASE MANAGEMENT*

by

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May 1982

An integrated computer system for image processing, pattern recognition, and pictorial database management will further advance state-of-the-art development of machine intelligence systems for advanced automation.

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*This research is supported in part by NSF grant ECS-80-16580, and in part by the Institute of Information Science, Academia Sinica.

Pattern analysis refers to the use of digital computers for Pattern Recognition and Image Processing (PRIP). On line imagery data needs to be stored on disks and fastly retrieved for PRIP applications. An effective pictorial information system requires both capabilities of efficiently managing and of fastly analyzing imagery data. This article presents a systematic approach to developing a special-purpose computer architecture for processing pictorial information. This approach integrates both pattern-analysis and image-database-management capabilities into a unified design for the said purposes. The integrated design is aimed at the development of a real-time and interactive computer system for processing multi-dimensional information.

A state-of-the-art assessment is presented on various pattern-analysis machines constructed or being reported in the literature. We shall examine special database machines suggested for handling imagery data. Recent efforts on VLSI hardware approaches to implementing PRIP algorithms and to processing image queries will be discussed. The integrated architectural approach is initiated by the PUMPS architecture currently under development at Purdue University[1,2]. We shall identify the desired architectural features, processing languages, image databases, and underlying VLSI computing structures for developing such intelligent computer systems.

PATTERN-ANALYSIS COMPUTERS

A typical pattern-analysis system consists of four processing stages as depicted in Fig.1. The filtering stage includes image operations like smoothing, enhancement, restoration, edge detection, and segmentation, etc. Raw images are reduced to segmented patterns by this initial stage. The second stage is for feature extraction, which further reduces the segmented image to a small set of feature vectors. Clustering techniques may be applied at this stage. The third stage is for pattern classification, which recognizes the membership of extracted features among known pattern classes. The fourth stage is for pattern understanding, which performs structural/texture analysis, shape discrimination, and 3-dimensional scene analysis to produce a brief description and precise interpretation of the pattern information[3,45,48,49,51].

Conventional Single-Instruction and Single-Data Stream (SISD) computers are primarily designed to process one-dimensional strings of alphanumerical data. To process multi-dimensional information on SISD computers requires image coding and picture transformation (such as projection, registration, etc.)[3]. Sequential machines cannot efficiently exploit parallelism embedded in most PRIP operations. On the other hand, large parallel computers, such as Single-Instruction Multi-Data Stream (SIMD) array processors and

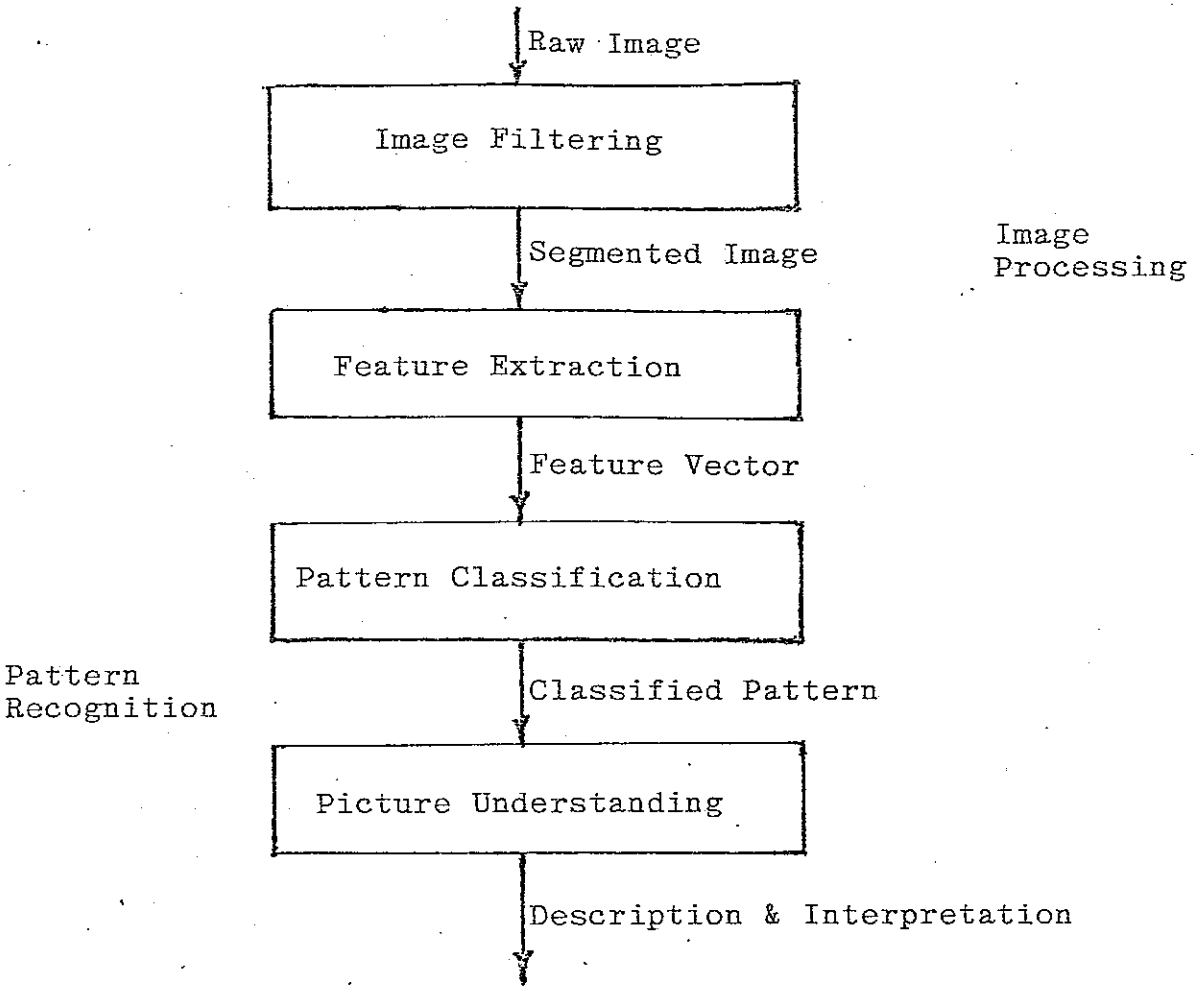

Fig.1 Processing stages of a pattern-analysis computer system

Multi-Instruction and Multi-Data stream (MIMD) multiprocessors, may not be necessarily cost-effective in implementing simple and repetitive image operations over very large and, sometimes, dynamically changing image databases.

An adequate pattern-analysis computer is expected to perform at least 100 megaflops with a memory bandwidth of at least 256 megabytes for applications in the 1980's, and many require to have processing power of 1000 megaflops or higher for those applications in the 1990's. Two excellent survey on special computer architectures for PRIP have been given by Fu[4] and by Danielsson and Levialdi[5].

ARCHITECTURAL REQUIREMENTS

Identified below are desired architectural characteristics and functional features of existing pattern-analysis computers. We focus on the interplay between computer architectures and PRIP applications. In general, a PRIP computer should be featured with as many of the following capabilities as possible:

(a) To explore spatial parallelism, a pattern-analysis computer may be equipped with replicated arithmetic/logic units operating synchronously in SIMD mode. Moreover, high degree of pipelining (temporal parallelism) is desired for overlapped instruction execution and pipelined vector arithmetic[6,47].

(b) Some PRIP computers choose a multiprocessor configuration to support asynchronous computations in MIMD mode. Data flow multiprocessor systems have been also suggested for PRIP or Artificial Intelligence computations[7].

(c) Hierarchical memory system is needed for image storage and manipulation. Large main memory with fast image cache must be employed to alleviate the problem of image data overflow. Fast and intelligent I/O and sensing devices are needed for interactive pattern analysis and image query processing[8].

(d) Special image database management systems or image database machines are demanded for fast image information retrieval. Toward this end, some high-level picture description/manipulation languages need to be developed, in addition to developing image query languages[9,10,11].

(e) PRIP computers should fully utilize state-of-the-art hardware component, and available software packages. Dedicated VLSI devices are needed for PRIP at signal-processing level and at symbol-manipulation level. Special VLSI pattern recognizers and image filtering chips are needed for fast image/picture construction, thresholding, FFT, histogram analysis, feature selection, and syntax analysis[12,13,14].

EXISTING SYSTEM ARCHITECTURES

The architectures of PRIP machines can be divided into three categories: SIMD array processors, pipelined vector processors, and MIMD multiprocessor systems. Summarized in Table 1 are various pattern-analysis computers, their architectural configurations, and reported applications.

The use of an SIMD array of Processing Elements (PEs) for solving spatial image problems has been realized in Illiac IV[15], STARAN[16], CLIP Series[17], and MPP[18]. In Illiac IV, image arrays structured other than 8 x 8 standard size must be partitioned into segmented loops in order to be properly processed by the 64 PE's. So far, Illiac IV has been applied for processing LANDSAT image, synthetic aperture radar signals, texture analysis, and linear programming image enhancement[19]. The STARAN is an associative processor with 256 PEs updating a multi-dimensional-access memory. STARAN has been applied in NASA's Large Area Crop Inventory Experiments (LACIE)[20], and in implementing a digital cartographic system for the Defense Mapping Agency[21]. CLIP IV is a cellular logic machine[22] with 96 x 96 bit-slice PE's. It is specially designed for parallel window and neighborhood operations. MPP is a bit-slice array processor with 128 x 128 PE's operating in lockstep. It is to be used mainly in processing satellite pictures for NASA[23].

Table 1. Summary of Pattern-Analysis Computers and Applications

Pattern Analysis Machine	Machine Architecture	Developer/ Constructor	Status/ References	Reported Applications
ILLIAC-IV	SIMD, 64 PE's connected by an Mesh 8 x 8 mesh network	Univ. of Illinois/ Burroughs Co.	Operational Since 1972. [15], [19]	Landsat Images, Sythetic Aperture Radar Signal Processing.
STARAN	SIMD, 32 arrays, 256 PE's per array, Associative, bit-slice structure, Flip Network.	Goodyear Aerospace Co.	Operational Science 1974 [16],[20], [21]	NASA's LACIE Experiments, Image Magnification, Convolution, Cartography for Defense Mapping Agency
CLIP-4	SIMD, bit-slice Cellular Mesh, 96 x 96 PE's. 8 Neighbors per PE, NMOS/LSI Circuits.	University College of London	Operational since 1976 [5],[9],[17], [22],[42],[51]	Window and Neighborhood Operations for Bit-Plan Image Processing and Feature Extraction.
MPP	SIMD, 128 x 128 PE's, Bit-Slice PE, RAM memory planes. Mesh Network, Custom VLSI Chips.	NASA/Goodyear Aerospace Co.	To be delivered to NASA in 1982, [5], [18],[23], [51]	Landsat Image Processing, Target Screening, Tactical Reconnaissance.
Cytocomputer	Pipelined with 88 processor stages of one type and 25 of another	Environmental Research Institute of Michigan	Under development as of 1982 [5], [8],[24],[27]	Cytology Analysis, Biomedical Image Processing
GOP	4 Arithmetic Pipes, with staged memory and Microprogram Control	Linkoeping Univ., Sweden	Under development as of 1982 [9], [25]	General Image Processing and Pattern Classification

Table 1. Summary of Pattern-Analysis Computers and Applications (continued)

Pattern Analysis Machine	Machine Architecture	Developer/ Constructor	Status/ References	Reported Applications
Systolic Processor	Systolic pipeline driven by a VAX-11/780 host	ESL/TRW, Advanced Processor Tech. Lab., San Jose	Under Construction 1982, [26]	Signal/Image Processing, 2-D Convolution and Resampling, FFT Operations
PICAP-II	Modular open-ended bus-structured Multiprocessor MIMD/SIMD	Linkoping University, Sweden	Basic System operational 1980, [5], [30]	Image Processing, Computer Graphics.
FLIP	16 Processors, MIMD, Recogfigurable Datapath Pipelines, Microprogrammable	Research Inst. for IPPR, Karlsruhe, West Germany	Under development as of 1982, [9], [33]	General image processing and pattern recognition
TOSPICS	Bus-structure multiprocessor system with declicated PRIP functions and fast image memory	Toshiba Co., Japan	Operational since 1978, [5],[31], [50]	Logical filtering, Region Labeling, Two-dimensional Convolution, Histogramming
ZMOB	256 micro-processors interconnected by pipelined bus, MIMD Mode	University of Maryland	Under Construction 1982 [5],[32], [34],[51]	Artificial Intelligence, Image Processing.
PUMPS	Multiprocessor system with shared functional device pool and backend image database machine	Purdue University	Under development as of 1982,[1], [2],[52]	Pattern Analysis, Image Processing, Image Database Management.

Pipelined machines for PRIP include the cytocomputer[24], the GOP[25], and the ESL/systolic processor[26]. The cytocomputer is highly pipelined with a bandwidth of 1.6M bytes per second over 113 pipeline stages. It was mainly designed for cytology analysis and biomedical image processing[27]. The GOP image processor, containing four computation pipelines, can work on grey-scale, color, or multisepctral images of various sizes. It has been applied in image filtering, edge/line detection, texture description, relaxation, and classification operations. The ESL/systolic processor is based on the systolic pipeline structure proposed by Kung and Leiserson[28]. It is developed for signal/image processing operations like multi-dimensional convolution and resampling[29].

Several MIMD multiprocessor systems were developed for PRIP applications. Among them are the PICAP-II[30], TOSPICS[31], ZMOB[32], FLIP[33], and PUMPS[1,52]. PICAP-II is a bus-structured multiprocessor. The bus allows 15 processors to be connected under the coordination of a host computer SEL 77/35. Some of the processors are themseleves SIMD array processors. The PICAP has been applied mainly in image processing research. TOSPICS is developed at Toshiba Corporation in Japan. It is also bus-structured with a number of dedicated processors for logical filtering, region labeling and two-dimensional convolution. A comprenhensive treatment of pattern recognition machines in Japan is given in the paper by Kidode[50].

ZMOB is under development at University of Maryland. It consists of 256 Zilog 80A 8-bit microprocessors. It is designed for artificial intelligence and general computer science research. So far, it has been planned for image operations like discrete transforms, geometric operations, and computation of image statistics[34]. The FLIP is an image multiprocessor suitable for window operations by 16 individual processors in either MIMD or SIMD mode under the control of a host machine. It can process a 512 x 512 image in about one second. PUMPS is an MIMD machine with an integrated architecture for pattern analysis and image database management.

IMAGE DATABASE MANAGEMENT

An image database system provides a large collection of structured imagery data (digitized pictures) for easy access by a large number of users. Existing image database systems and their reported applications are summarized in Table 2. Most of these image database systems are implemented with specially developed software packages upon dedicated pattern analysis systems. Interested readers may refer to references 10,11,35,36,37 for some details of these systems. It is highly desirable to develop a dedicated backend database machine for image database management. Several hardware attempts were suggested[1,38,39]. But none of them has been implemented yet.

Table 2. Summary of Image Database Systems and Reported Applications

Image Database System	Developer, Year of Introduction, and Reference	Implementation Approach and Capabilities	Reported Key Applications
IBIS	Bryant/Zobrist, Jet Propulsion Laboratory, 1977, [36]	Built upon existing VICAR image analysis system, Vedio Image Communication and retrieval	Pictorial information processing of LANDSAT data for geographic analysis
IMAID	Chang/Fu, Purdue University, 1978, [10]	Relational model, using Query-by-Pictorial Examples, interfaced with an image analysis system and spatial operators	Picture Manipulation, and similarity retrieval for research on advanced pattern analysis and automation
CGIS	Tomlinson, Canadian Environmental Department, 1968, [53]	Use command and assessment languages, Overlapping of maps, interactive graphics, polygon representation	Geographic information processing and regional planning
GADS	Mantey/Carlson, IBM, San Jose, 1979, [54]	Relational model, built-in relational operators, interactive data access.	Geodata analysis and display system
MIDAS	McKeown/Reddy, 1977,[55]	Hierarchical model, a multisensor image database system	Image understanding and knowledge acquisition
GEQ-QUEL	Berman/Stonebracker, University of California at Berkeley, 1977, [56]	Relational model, integrated with INGRES database system using QUEL query language	Manipulate geographic data
GRAIN	Chang/Reduss/McCormick, University of Illinois at Chicago Circle 1977, [57]	Relational database with hierarchical structure, Various image retrieval functions Logical zooming, algebraic interpretation	Pictorial information retrieval and manipulation, knowledge system research
SID	Kunii/Harada University of Tokyo, 1980, [58]	Relational model, Interactive design using recensively structured graphs.	Computer-Aided Design (CAD) of software and electronic circuits and engineering drawing evolution
IMDS	Lien/Utter, University of Kensas, 1977, [59]	Relational model, Using IQ command language store both image and image registrations	Image retrieval and query language research
POLYVRT	Chrisman/Little, Harvard University 1978, [60]	A polygon approach through line segment chaining. Overlay and Merge functions	Research on Computer graphics and spatial analysis

VLSI PRIP ALGORITHMS

Recent advances in VLSI micro-electronic technology has triggered the thought of implementing some PRIP algorithms directly in hardware. VLSI pattern recognizers offer high speed and accuracy which are useful in real-time, on-line, pictorial information processing. This is the first step towards advanced automation and machine intelligence. Recently, many attempts have been made in developing special VLSI devices for signal/image processing and pattern recognition[12,13,14,26,29,40,41,42]. Most of these approaches involve large-scale matrix computations or syntatic parsing operations. We list in Table 3 some candidate PRIP algorithms that might be suitable for VLSI implementation.

Two concrete design examples are presented below to illustrate the VLSI approaches to high-speed pattern recognition and image analysis. The first example presents some matrix manipulation networks for statistical feature extraction. The second example shows a two-dimensional pipeline for fast recognition of context-free languages. "Partitioned" matrix algorithms[43] can be applied for VLSI L-U decomposition, matrix multiplication, matrix inversion, and solving triangular systems of equations. Pipelined VLSI networks have been developed to realize these partitioned matrix algorithms[12]. Figure 2 shows the functional design of a pipelined VLSI matrix inverter.

Table 3. Pictorial Information Processing Algorithms for Possible VLSI Implementation

Image Processing	Enhancement, Filtering, Fhining, Edge Detection, Segmentation, Registration, Restoration, Clustering, Texture Analysis, Convolution, Fourier Analysis, etc.
Pattern Recognition	Feature Extraction, Template Matching, Statistical Classification, Graph Algorithms, Syntax Analysis, Change Detection, Language Recognition, Scene Analysis and Synthesis, etc.
Image Query Processing	Query Decomposition, Query Optimization, Attribute Manipulation, Picture Reconstruction, Search/Sorting Algorithms, Query-by-Picture-Example Implementation, etc.
Image Database Processing	Relational Operators (JOIN, UNION, INTERSECTION, PROJECTION, COMPLEMENT), Image-Shetch-Relation Conversion, Similarity Retrieval, Data Structures, Priority Queues, Dynamic Programming, Spatial Operators, etc.

$$U^{-1} = \begin{pmatrix} U_{11} & U_{12} & U_{13} & U_{14} \\ 0 & U_{22} & U_{23} & U_{23} \\ 0 & 0 & U_{33} & U_{34} \\ 0 & 0 & 0 & U_{44} \end{pmatrix}^{-1} = \begin{pmatrix} V_{11} & V_{12} & V_{13} & V_{14} \\ 0 & V_{22} & V_{23} & V_{24} \\ 0 & 0 & V_{33} & V_{34} \\ 0 & 0 & 0 & V_{44} \end{pmatrix} = V$$

All U_{ij} and V_{ij} are m × m submatrices. U and V are both n × n
The case of k = n/m = 4 is shown.

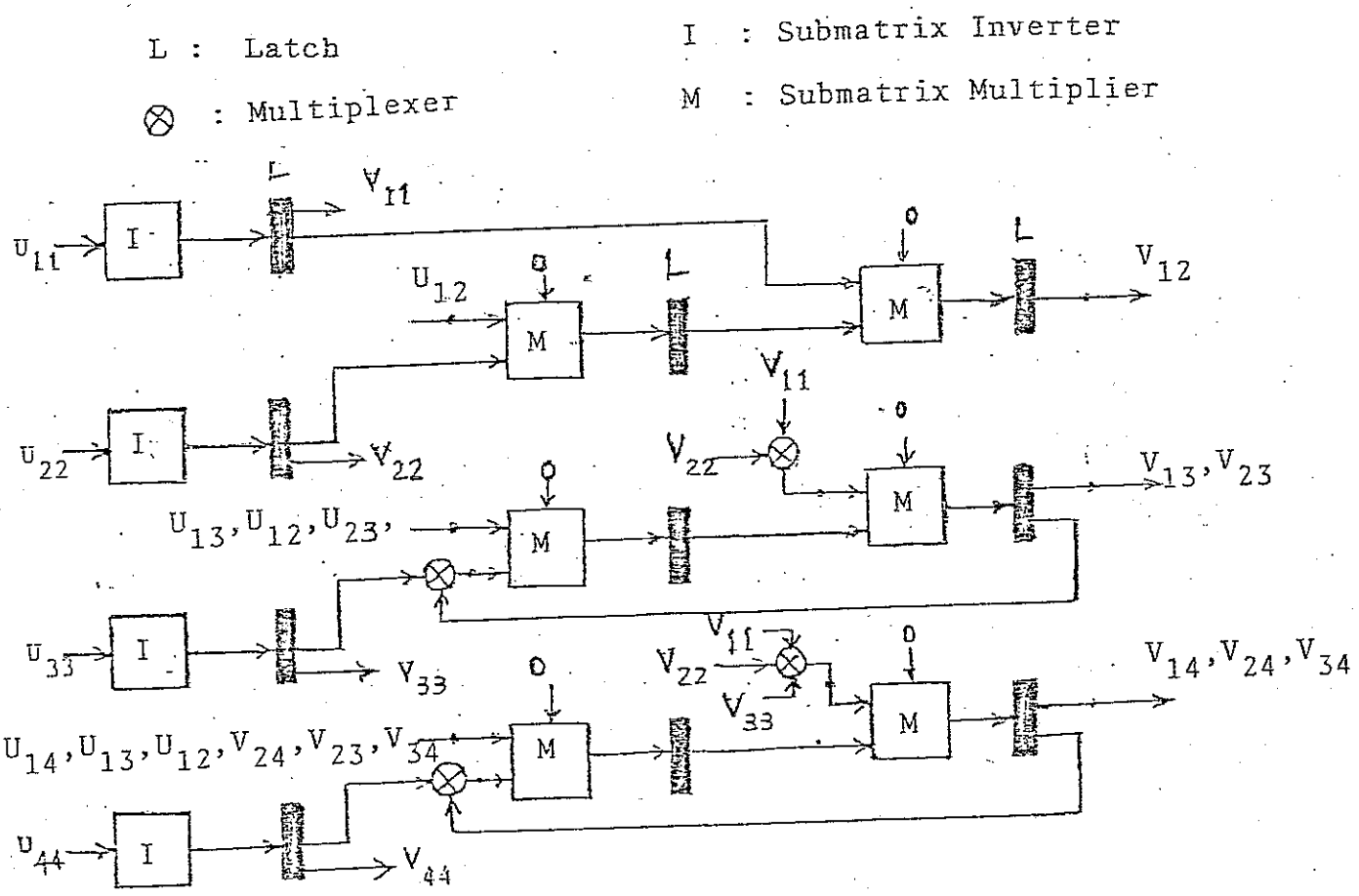

Fig.2 VLSI Architecture for pipelined matrix inversion

Each square block shown in Fig. 2 corresponds to a VLSI matrix arithmetic device for handling submatrix computations. The input is an n x n upper triangular matrix U partitioned into k^2 submatrices of dimension m x m such that $n = k \cdot m$. The case of $k = n/m = 4$ is shown in Fig.2. Listed below are required submatrix computations in four sequential steps to generate the inverse matrix V in a partitioned fashion. Note that U_{ij} and V_{ij} are m x m submatrices and U_{ii} and V_{ii} are upper-triangular submatrices.

Partitioned Matrix Inversion (for the case of $k = n/m = 4$).

Step 1. $V_{ii} = U_{ii}^{-1}$ for $i = 1,2,3,4$

Step 2. $V_{i,i+1} = -V_{ii} \cdot (U_{i,i+1} \cdot V_{i+1,i+1})$ for $i = 1,2,3$

Step 3. $V_{i,i+2} = -V_{ii} \cdot (U_{i,i+1} \cdot V_{i+1,i+3} + U_{i,i+2} \cdot V_{i+2,i+2})$; for $i = 1,2$

Step 4. $V_{14} = -V_{11} \cdot (U_{12} \cdot V_{24} + U_{13} \cdot V_{34} + U_{14} \cdot V_{44})$

The I-modules are used to perform the inversion of the m x m upper-triangular submatrices at Step 1. The M-modules are used to perform the cumulative matrix multiplications specified in Step 2 through Step 4. The inputs and outputs at four successive computation steps are indicated at the I/O terminals in Fig.2. In general, inverting an n x n triangular matrix using this VLSI pipeline requires to use k I-modules and 2(k - 1) M-modules. Thus the total VLSI module count equals $O(k) = O(n/m)$ for $n >> m$. The

total time delay to generate $V = U^{-1}$ equals $O(n^2/m)$ for $n >> m$. An application of these VLSI matrix manipulation networks is shown in Fig.3 for the construction of a hardware feature extractor based on Foley and Sammon's algorithm[44]. The network subsystems for matrix multiply, L-U decomposition, and training sample manipulation can be similarly constructed with aforementioned VLSI arithmetic modules. Details of these VLSI matrix solvers can be found in[12,43].

A VLSI pipelined array for high-speed recognition of context-free languages is shown in Fig.4.a. This pipelined array can be applied in syntactic pattern recognition[45]. The array is constructed with $n(n + 1)/2$ processing cells, each of which assumes the functional structure shown in Fig.4.b. This two-dimensional array can recognize any input string of length n in 2n time units. The recognition process is based on the Cocke-Kasami-Younger algorithm. Details of this context-free language recognizer and its extension to recognize finite-state languages can be found in Ref.14. Similar VLSI approaches can be extended to other PRIP algorithms as listed in Table 3, including some for image query language processing and image database operations.

THE INTEGRATED ARCHITECTURE

The three functions, image processing pattern recognition, and image database management, must be integrated into an efficient pictorial information system. A data-flow block diagram of such an integrated system is shown in Fig.5. Three subsystems

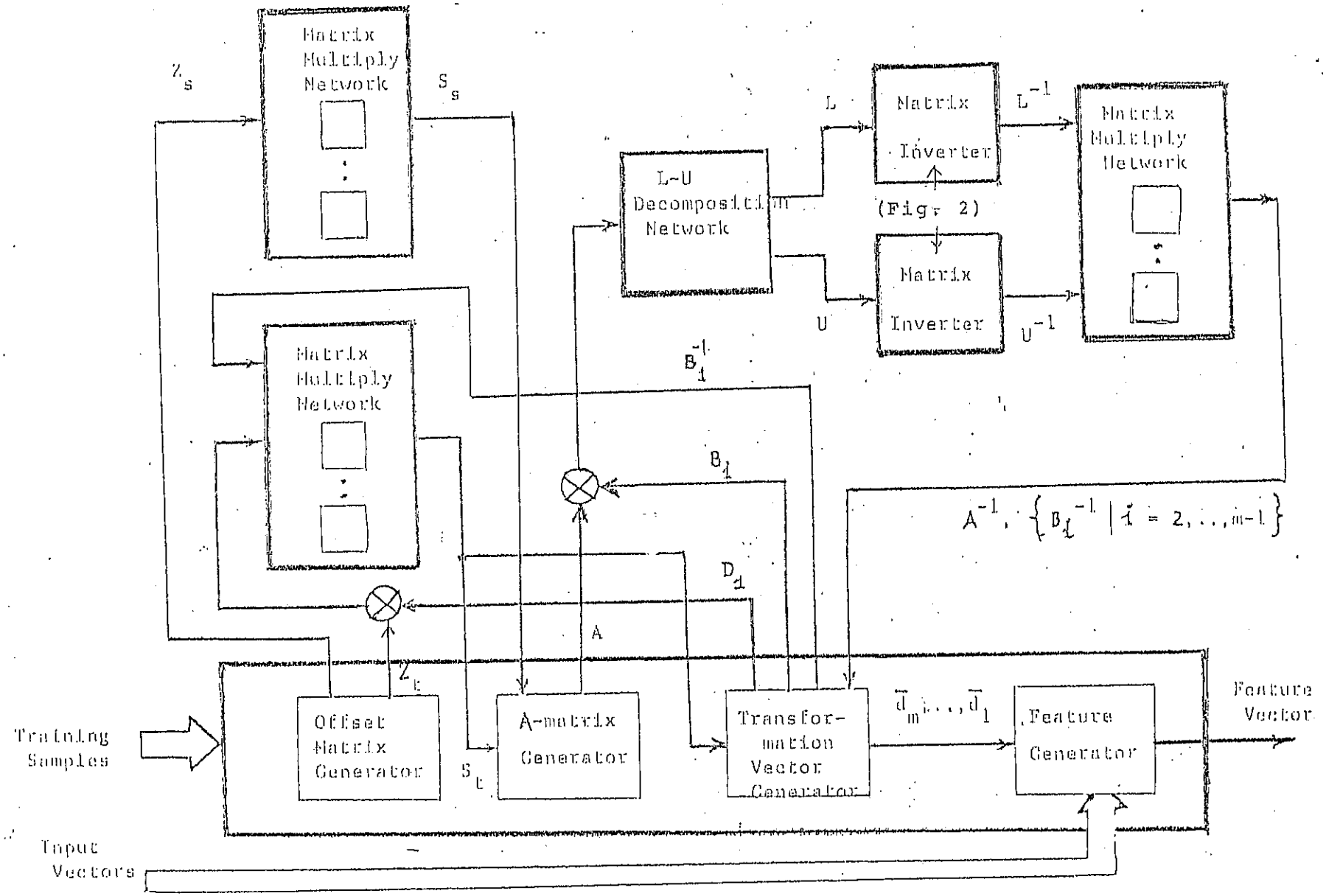

Fig.3 VLSI Matrix manipulation network for statistical feature extraction

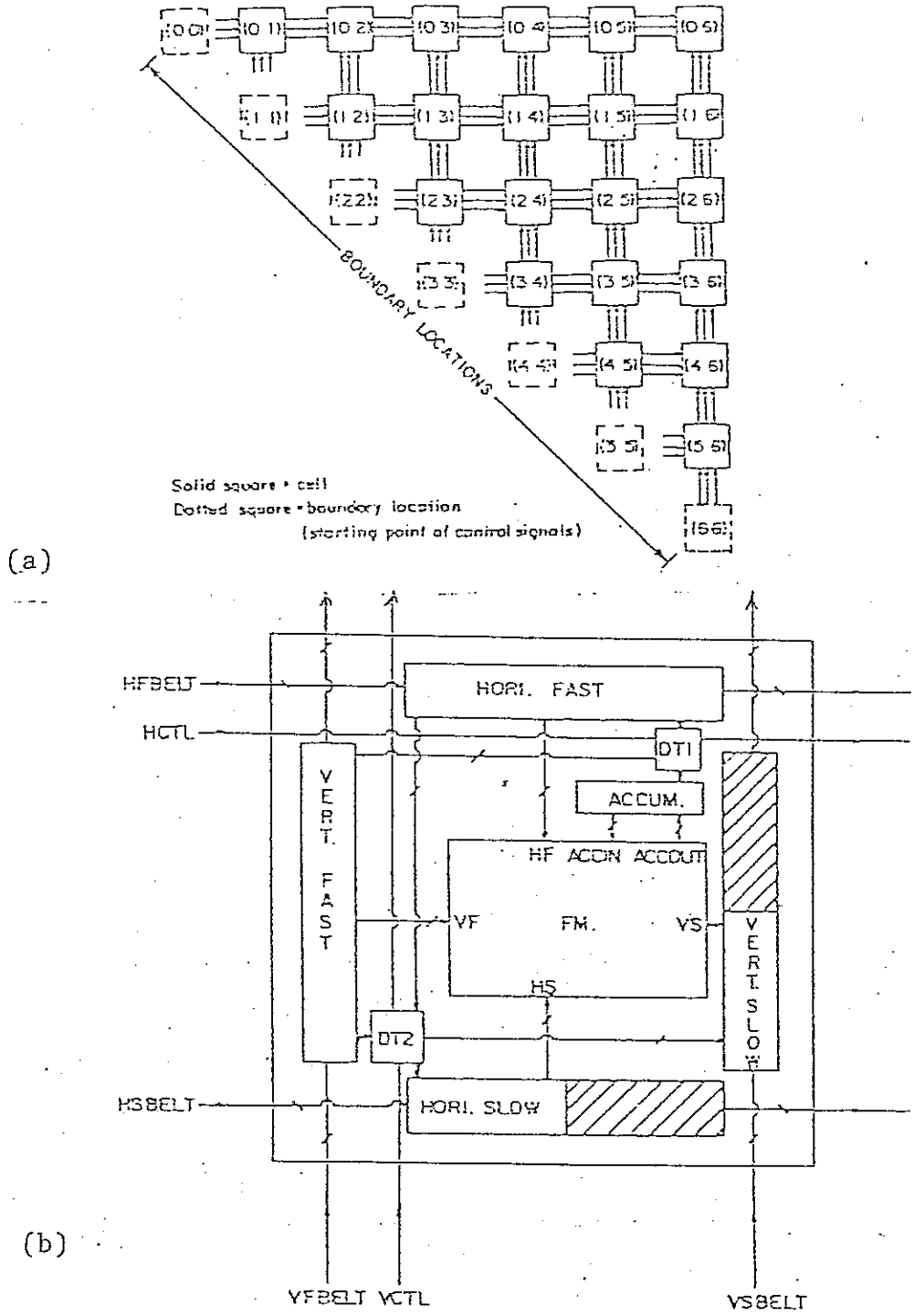

Fig.4 VLSI architecture for fast recognition of context-free languages

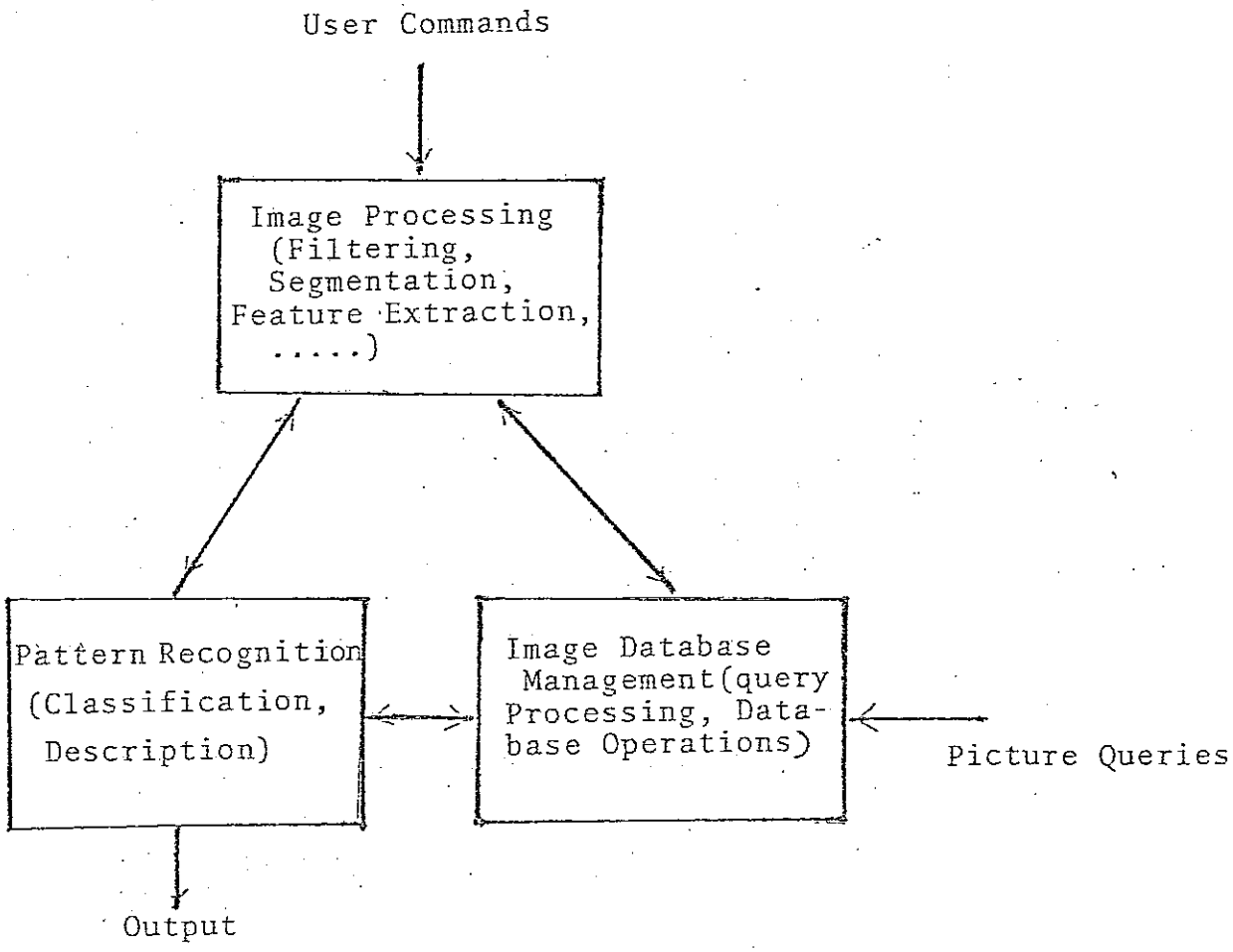

Fig.5 Data flow diagram of an integrated computer system for pattern analysis/image database management

correspond to the three addressed functions. These subsystems must interact and cooperate with each other to achieve the said objectives. The user communicates with the system through some pictorial query language. The raw images are physically stored on disks (or tapes). A relational image database is established by mapping the physical images into the logically structured database. The image processing subsystem performs image filtering and feature extraction. The pattern recognition subsystem performs pattern classification and picture understanding operations. The image management subsystem handles query processing and image database operations.

The system architecture of such an integrated picture processing computer is conceptually illustrated in Fig.6. The system consists of four major subsystems, as shown by the major blocks in the drawing. The host computer can be any one of those pattern-analysis computers listed in Table 1. The backend database machine is specially developed for image database management. Either software or hardware approaches can be adopted in developing image database management systems as summarized in Table 2. The front-end communication processor is used to handle terminal activities or to be connected to a computer network for remote users. The shared resource pool contains VLSI functional units or attached special processors for fast PRIP operations as examplified in Table 3. A resource arbitration network is needed between the host processors and the shared resource pool.

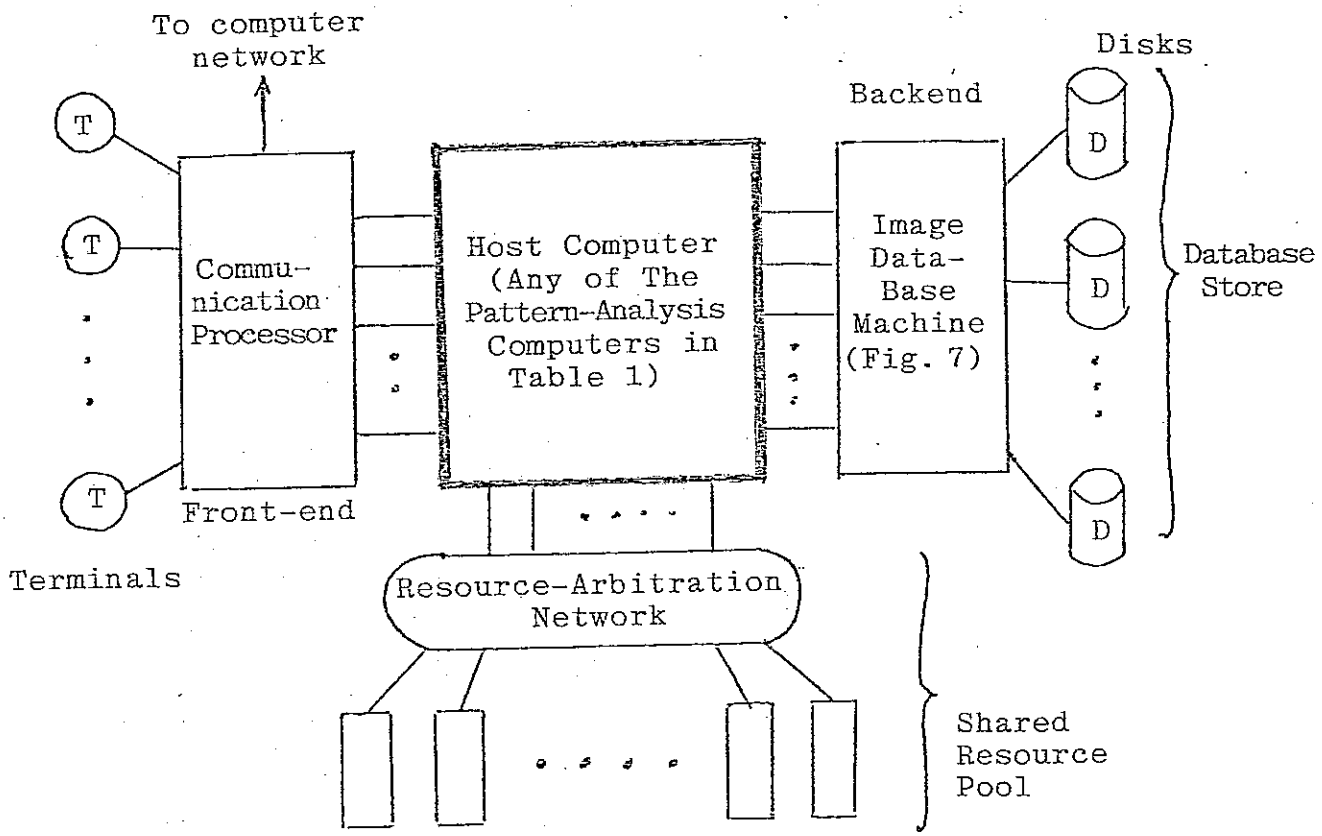

Fig.6 Architecture of the integrated computer system for pattern analysis and image database management

One of the attempts to realize such an integrated computer system is the PUudue MultiProcessor System (PUMPS) architecture [20]. The host computer in PUMPS is a multiprocessor system which can operate in either MIMD mode or in Multiple-SIMD mode or Multiple-SISD mode. The detailed system architecture of PUMPS has been presented in Ref.1. The system host consists of n uniprocessors sharing m memory modules through an Inter-Processor-Memory Network. The resource pool of special-purpose VLSI functional units and peripheral processors is shared by all n processors. The database machine can directly transfer information from the database store (disks) to the shared memory modules in PUMPS. Special VLSI devices in the resource pool can be dynamically allocated to multiple processors in the host system for carrying out its assigned functions. They can be also cascaded together as a dynamic pipeline for chained vector operations. Shared cache memories can be also used between the local processor memories and the shared memories in order to facilitate MIMD operations.

Presented in Fig.7 is a back-end image database machine. It is itself a multiprocessor system for parallel query processing and image database management. This structure is very similar to the DIRECT architecture[46], with multiple query processors accessing a set of shared data banks. We add a set of VLSI database functions that can be shared by the parallel query processors. Again, a resource sharing network is needed between the query processors and shared VLSI database operators. The shared database operators could be used for data filtering, projection, join or other operations if relational image database is established. Some VLSI database operators were listed in Table 3.

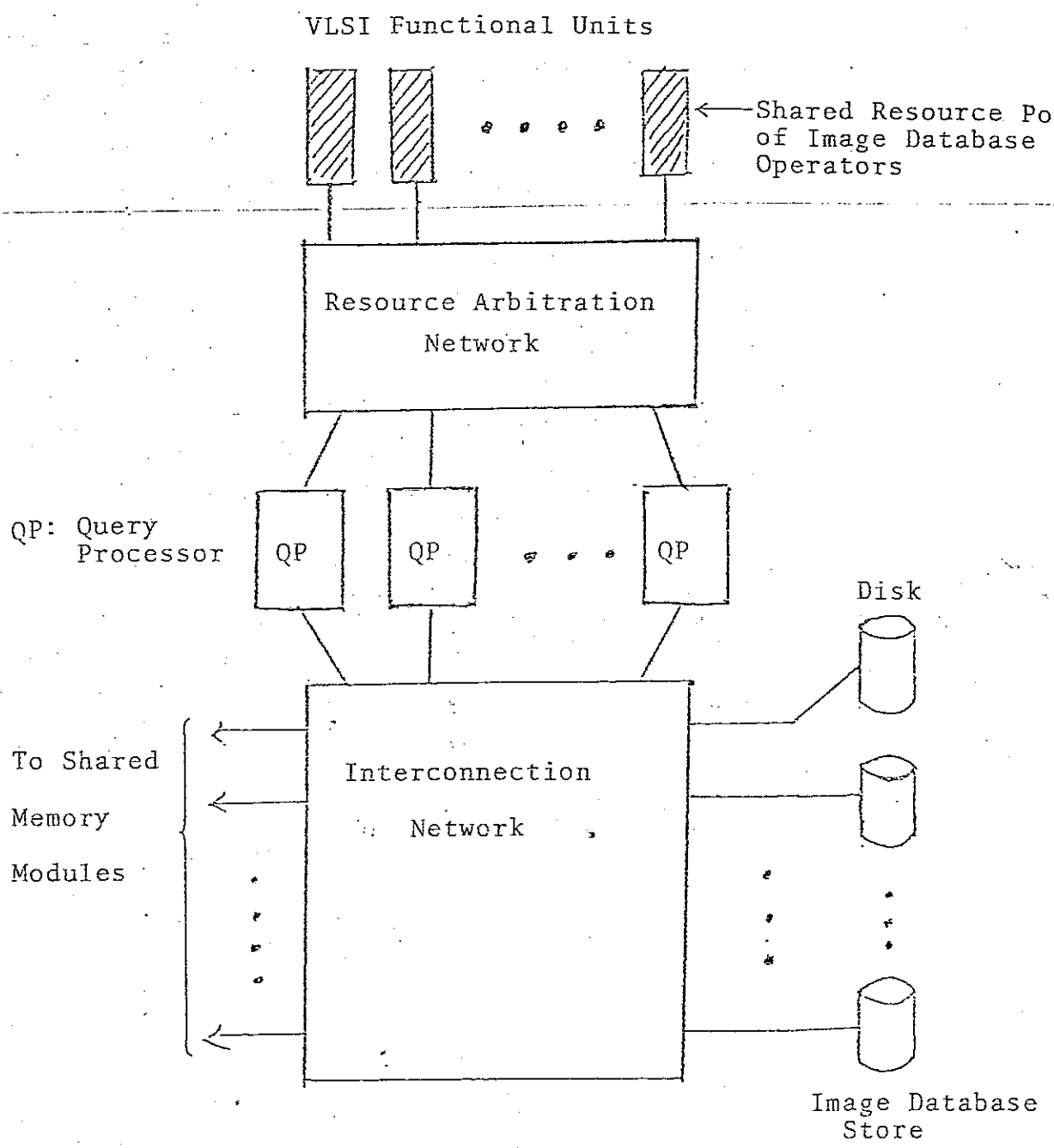

Fig.7 A multiprocessor image database machine with shared resource pool of VLSI Database Manipulators

CONCLUSIONS

After examining existing pattern-analysis computers and image database systems, the system designer can easily realize the fact that the two addressed functions cannot be separated in an efficient pictorial information system. The integrated system approach is well supported by the merging VLSI technology and VLSI computing structures. Cost-effectiveness is the key issue in developing special-purpose machines for image processing, recognition, and database management. Such integrated computer architecture will further advance state-of-the-art development of machine intelligence systems for advanced automation, knowledge processing, and artificial intelligence.

REFERENCES:

[1] Briggs, F. A., Hwang, K., Fu, K. S., and B. W. Wah, "PUMPS Architecture for Pattern Analysis and Image Database Management," Proc. Workshop Comp. Arch. for PAIDM, Hot Springs, Virginia, 1981, pp.178-187.

[2] Fu, K. S. and Chang, N. S., "An Integrated Image Analysis and Image Database Management System," Proc. COMPCON, Fall, 1982.

[3] Rosenfeld, A. and Kak, A. C. Digital Picture Processing, Academic Press, New York, 1976.

[4] Fu, K. S., "Special Computer Architectures for Pattern Recognition and Image Processing," Proc. of National Computer Conf., Vol. , AFIPS Press, 1978, pp.1003-1013.

[5] Danielsson, P. E. and Levialdi, S., "Computer Architectures for Pictorial Information Systems," Computer, IEEE Computer Society, November 1981, pp.53-67.

[6] Hwang, K., Su, S. P. and Ni, L. M. "Vector Computer Architecture and Processing Techniques," in Advances in Computers, Vol.20 (Yovits, Ed.) Academic Press, 1981, pp.115-197.

[7] Amamiya, M., Hasegawa, R., and Mikami, H., "List Processing on A Dataflow Machine", in Research Reports in Japan, The Fifth Generation Computer Project, JIPDEC, Tokyo 105, Japan, Fall 1981, pp. 149-183.

[8] Onoe, M., Preston, K., and Rosenfeld, A. (Editors), Real-Time/Parallel Computing: Image Analysis, Plenum Press, N.Y. 1981.

[9] Duff, M. J. and Levialdi, S. (Editors), Languages and Architectures for Image Processing, Academic Press, N. Y., 1981.

[10] Chang, N. S. and Fu, K. S., "Picture Query Languages for Pictorial Database Systems, " IEEE Computer Magazine, Nov. 1981, pp.23-33.

[11] Chang, S. K. and Kunii, T. L., "Pictorial Database Systems," IEEE Computer Magazine, Nov. 1981, pp.13-22.

[12] Hwang, K. and Su, S. P., "VLSI Matrix Manipulators for Feature Extraction and Pattern Classification," TR-EE81- , School of E. E., Purdue Univ., Lafayette, Indiana (submitted for publication).

[13] Yang, T. Y. and Liu, P. S., "VLSI Arrays and Control Structure for Image Processing, "in Proc. Workshop Comp. Arch. for PAIDM, Hot Springs, 1981, pp.257-264.

[14] Chu, K. H. and Fu, K. S., "VLSI Architectures for High-Speed Recognition of General Context-Free Languages and Finite-State Languages," TR-EE 81-42, Purdue University, 1981. (Submitted for publication).

[15] Barnes, G. H., Brown, R. M., Kato, M., Kuck, D. J., and Stokes, R. W., "The Illiac IV Computer," IEEE Trans. Computers, Vol.C-17, 1968, pp.746-

[16] Rohrbacher, D. and Potter, J. L., "Image Processing with STARAN Parallel Computer," IEEE Computer Magazine, August 1977, pp.54-59.

[17] Duff, M. J. B., "Review of the CLIP Image Processing System," Proc. of NCC, Vol.47, AFIPS Press, 1978, pp.1055-1060.

[18] Batcher, K. E., "Design of a Massively Parallel Processor," IEEE Trans. Computers, Vol.C-29, Setp. 1980, pp.836-840.

[19] Hord, R. M. and Stevenson, D. K., "The Illiac IV Architecture and Its Sutiability For Image Processing," in Special Computer Architecture for Pattern Recognition, (Fu and Ichikawa, Editors), Chap.6, CRC Press, 1982, pp.

[20] Faiss, R. J., Quinn, L. M., and Ruben, S., "Application of A Parallel Processing Computer in LACIE," Proc. 1976 Int'l Conf. Parallel Processing, pp.24-32.

[21] Potter, J. L., "Pattern Processing on STARAN," in Special Computer Architecture for Pattern Recognition, (Fu and Ichikawa, Editors), Chap.5, CRC Press, 1982, pp.

[22] Duff, M. J., "CLIP 4," in Special Computer Architecture for Pattern Recognition, (Fu and Ichikawa, Editors), Chap.4, CRC Press, 1982, pp.

[23] Potter, J. L., "Image Processing on The Massively Parallel Processor", This issue.

[24] Lougheed, R. M., McCubbrey, D. L., and Sternberg, S. R., "Cytocomputers: Architectures for Parallel Image Processing," Proc. Workshop Picture Data Description and Management, August 1980, pp.281-286.

[25] Grandlund, G. H., et al., "The GOP IMage Processor," Proc. Workshop Comp. Arch. for Pattern Analysis and Image Database Management, IEEE Computer Society, 1981, pp.195-200.

[26] Yen, D. W. L., and Kulkami, A. V., "The ESL Systolic Processor for Signal and Image Processing," Proc. Workshop Comp. Arch. for PAIDM, Hot Springs, Virginia, 1981, pp.265-272.

[27] Sternberg, S. R., "Cytocomputers and Biomedical Image Processing", This issue.

[28] Kung, H. T. and Leiserson, "Systolic Arrays (for VLSI)," in Sparse Matrix Proc. (Duff and Stewart, Eds), 1979, pp.256-282.

[29] Kung, H. T. and Picard, R. L., "Hardware Pipelines for Multi-Dimensional Convolution and Resampling," Proc. Workshop Comp. Arch. for PAIDM, Hot Springs, 1981, pp.273-278.

[30] Antonsson, D., et al., "PICAP — A System Approach to Image Processing," Proc. Workshop Comp. Arch. for PAIDM, Hot Springs, Virginia, 1981, pp.35-42.

[31] Mori, K. I., Kidode, M., and Shinoda, H., and Asada, H., "Design of Local Parallel Pattern Processor for Image Processing," Proc. of NCC, Vol.47, AFIPS Press, 1978, pp.1025-1031.

[32] Rieger, C., "ZMOB : Doing It in Parallel," in Proc. Workshop Comp. Arch. for PAIDM, Hot Springs, Virginia, 1981, pp.119-124.

[33] Luetjen, K., Gemmar, P., and Ischen, H., "Flip : A Flexible Multiprocessor System for Image Processing," Proc. 5th Int'l Conf. Pattern Recognition, Miami Beach, Fla., 1980, pp.326-328.

[34] Kushner, T., Wu, A. Y. and Rosenfeld, A., "Image Processing on ZMOB," Proc. Workshop Comp. Arch. for PAIDM, Hot Springs, 1981, pp.88-95.

[35] Yamamura, M., Kamibayashi, N., and Ichikawa, T., "Organization of An Image Database Manipulation System," Proc. Workshop Comp. Arch. for PAIDM, Hot Springs, 1981, pp.236-241.

[36] Zobrist, A. L. and Nagy, G., "Pictorial Information Processing of Landsat Data for Geographic Analysis", Computer, IEEE Computer Society, Nov. 1981, pp. 34-41.

[37] Chock, M., Carderas, A. F., and Klinger, A., "Manipulating Data Structures in Pictorial Information Systems", Computer, IEEE Computer Society, Nov. 1981, pp. 43-50.

[38] Wah, B. W. and Yao, S. B., "DIALOG — A Distributed Processor Organization for Database Machine," Proc. of NCC, Vol.49, AFIPS Press, 1980, pp.243-255.

[39] Hurson, A., "An Associative Backend Machine for Database Management," Proc. Workshop Comp. Arch. for PAIDM, Hot Springs, Virginia, 1981, pp.225-230.

[40] Chang, N. S. and Yuan, Y. C., "VLSI Design and Verification of a Signal Processing Chip," Proc. Workshop Comp. ARch. for PAIDM, Hot Springs, 1981, pp.279-283.

[41] Swartzlander, E., "VLSI Architecture," in VLSI : Fundamentals and Applications, (Barbe, Ed.) Springer Verlag, N. Y., 1980.

[42] Preston, K., Duff, M. J., Levialdi, S., Norgren, P. E., and Toriwaki, J. I., "Basis of Cellular Logic With Some Applications in Medical Image Processing," IEEE Proceedings, Vol.67, May 1979, pp.826-856.

[43] Hwang, K. and Cheng, Y. H. "Partitioned Matrix Computations for VLSI Arithmetic Systems", accepted to appear IEEE Transactions on Computer, 1982.

[44] Foley, D. H. and Sammon, J. W., "An Optimal Set of Discrimiant Vectors," IEEE Trans. Computer, March 1975, pp.281-289.

[45] Fu, K. S., Syntactic Methods in Pattern Recognition, Academic Press, N. Y., 1974.

[46] DeWitt, T., "DIRECT: A Multiprocessor Database Machines," IEEE Trans. Computers, 1977.

[47] Hwang, K., Computer Arithmetic: Principles, Architecture, and Design, John Wiley, 1979.

[48] Fu, K. S., Syntatic Pattern Recognition and Applications, Prentice-Hall, Englewood Cliffs, N. J., 1981.

[49] Fukunaga, K. Introduction To Statistical Pattern Recognition, Academic Press, N. Y. 1972.

[50] Kidode, M., "Pattern Recognition Machines in Japan", This issue.

[51] Rosenfeld, A., "Cellular Architectures For Pattern Recognition", This issue.

[52] Briggs, F. A., M. Dubois, and K. Hwang, "Throughput Analysis and Configuration Design of A Shared-Resource Multiprocessor System: PUMPS", Proc. of 8th Annual Symposium on Computer Architecture, IEEE Computer Society, May 1981, pp. 67-80.

[53] Tomlinson, R. "A Geographic Information System For Regional Planning", in Land Evaluation, (Ed. by Stewart), McMillan, Sydney, 1968.

[54] Mantey, P. E. and Carlson, E. D., "Integrated Geographic Data Bases: The GADS Experience", in Data Base Techniques for Pictorial Applications, (Ed. by Blaser), Springer-Verlag, 1979, pp. 173-198.

[55] McKeown, D. M. and Reddy, D. J., "A Hierarchical Symbolic Representation for Image Databases", Proc. IEEE Workshop Picture Data Description and Management, April 1977, pp. 40-44.

[56] Berman, R. and Stonebraker, "GEO-QUEL: A System for The Manipulation and Display of Geographic Data", Computer Graphics, Vol. 11, No. 2, 1977, pp. 186-191.

[57] Chang, S. K., Reuss, J. and McCormick, "Design Considerations of a Pictorial Database System", Int'l Journal of Policy Analysis and Information Systems, Vol. 1, No. 2, Jan. 1978, pp. 49-70.

[58] Kunii, T.L. and Harada, M. "SID: A System for Interactive Design", AFIPS Conf. Proc., 1980 NCC, May 1980, pp. 33-40.

[59] Lien, Y. E. and Utter, D. F., "Design of an Image Database", Proc. IEEE Workshop Picture Data Description and Management, April 1977, pp. 131-136.

[60] Chrisman, N. and Little, J., "POLYVRT 1.1" Harvard University Int'l User's Conf. Computer Mapping Software and Databases, 1978.